AMENDMENTS TO CLAIMS

- Please cancel claims 1, 3-11, and 13-15 without prejudice.

Claims 1-15. (cancelled)

16. (previously presented) An integrated circuit comprising:
a semiconductor substrate;
a gate dielectric on the semiconductor substrate;
a gate on the gate dielectric;
source/drain junctions in the semiconductor substrate;
a silicide on the source/drain junctions and on the gate;
an insulating liner around the gate;
an insulating film over the insulating liner;
trenches in the semiconductor substrate at the outer edges of the insulating film;
an interlayer dielectric above the semiconductor substrate; and
contacts in the interlayer dielectric to the silicide.

17. (cancelled)

18. (original) The integrated circuit as claimed in claim 16 wherein:
the trenches extend into the semiconductor substrate to a level lower than the silicide.

19. (original) The integrated circuit as claimed in claim 16 wherein:
the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

20. (original) The integrated circuit as claimed in claim 16 wherein:
the contacts to the silicide comprise materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

21. (previously presented) A method of forming an integrated circuit comprising:
providing a semiconductor substrate;
forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming a sidewall spacer around the gate;

forming a cusp at the outer edge of the sidewall spacer;

removing the sidewall spacer at the cusp;

forming source/drain junctions in the semiconductor substrate;

forming a silicide on the source/drain junctions and on the gate;

forming trenches in the semiconductor substrate at the outer edge of the sidewall spacer;

forming an interlayer dielectric above the semiconductor substrate; and

forming contacts in the interlayer dielectric to the silicide.

22. (previously presented) The method as claimed in claim 21 wherein:

forming the trenches uses an etching process that etches the semiconductor substrate.

23. (previously presented) The method as claimed in claim 21 wherein:

forming the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

24. (previously presented) The method as claimed in claim 21 wherein:

forming the contacts to the silicide uses materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.